

CLAIMS

What is claimed is:

1. A latch circuit with a metastability trap comprising:
 - at least three input latches each having an input terminal for receiving an input signal, a clock terminal for receiving a first clock signal, and an output terminal, said at least three input latches latching values of said input signal compared to at least three corresponding different threshold voltages at a predetermined point in time to provide at least three corresponding latched values;
 - a first logic gate having input terminals coupled to corresponding output terminals of each of said at least three input latches, and an output terminal for providing a first intermediate signal, said first logic gate activating said first intermediate signal in response to signals at all of said input terminals being in a first logic state, and keeping said first intermediate signal inactive otherwise;
 - a second logic gate having input terminals coupled to corresponding output terminals of each of said at least three input latches, and an output terminal for providing a second intermediate signal, said second logic gate activating said second intermediate signal in response to signals at all of said input terminals being in a second logic state, and keeping said second intermediate signal inactive otherwise; and
 - a flip-flop having a set input terminal coupled to said output terminal of said second logic gate, a reset terminal coupled to said output terminal of said first logic gate, and an output terminal for providing an output signal of the latch circuit.
2. The latch circuit of claim 1 further comprising a final stage latch having a data input terminal coupled to said output terminal of said flip-flop, a clock input terminal for receiving a capture clock signal, and an output terminal for providing a second output signal of the latch circuit.

3. The latch circuit of claim 2 wherein said capture clock signal is substantially complementary to said first clock signal.
4. The latch circuit of claim 1 wherein each of said at least three input latches comprises a clocked D-type flip-flop.
5. The latch circuit of claim 1 wherein said first logic state is a logic zero and said second logic state is a logic one.
6. The latch circuit of claim 5 wherein said first logic gate comprises a NOR gate.
7. The latch circuit of claim 5 wherein said second logic gate comprises an AND gate.
8. The latch circuit of claim 1 wherein said flip-flop comprises an SR-type flip-flop.
9. A latch circuit with a metastability trap comprising:
 - means for latching values of an input signal compared to at least three different threshold voltages at a predetermined point in time to provide at least three corresponding latched values;
 - a first logic gate having input terminals for receiving respective ones of said at least three corresponding latched values, and an output terminal for activating a first intermediate signal when all of said at least three corresponding latched values are in a first logic state, and for keeping said first intermediate signal inactive otherwise;
 - a second logic gate having input terminals for receiving respective ones of said at least three corresponding latched values, and an output terminal for activating a second intermediate signal when all of said at least three corresponding latched values are in a second logic state,

and for keeping said second intermediate signal inactive otherwise;
and

output means coupled to said first logic gate and to said second logic gate for changing an output signal to a first logic state in response an activation of said second intermediate signal, for changing said output signal to a second logic state in response to an activation of said first intermediate signal, and for maintaining a logic state of said output signal when both said first intermediate signal and said second intermediate signal are inactive.

10. The latch circuit of claim 9 further comprising second output means for periodically capturing said output signal to provide a second output signal.
11. The latch circuit of claim 10 wherein said second output means comprises a clocked D-type flip-flop.
12. The latch circuit of claim 9 wherein said means for latching comprises at least three clocked D-type flip-flops.
13. The latch circuit of claim 9 wherein said first logic state is a logic zero and said second logic state is a logic one.
14. The latch circuit of claim 9 wherein said output means comprises an SR-type flip-flop.

15. A method for trapping metastability events to provide a metastable-free output signal, comprising the steps of:
 - latching values of an input signal compared to at least three different threshold voltages at a predetermined point in time to provide at least three corresponding latched values;
 - activating a first intermediate signal when all of said at least three corresponding latched values are in a first logic state;
 - activating a second intermediate signal when all of said at least three corresponding latched values are in a second logic state;
 - placing an output signal in a first predetermined logic state in response to said second intermediate signal; and
 - changing said output signal from said first predetermined logic state to a second predetermined logic state in response to said first intermediate signal.
16. The method of claim 15 further comprising the step of periodically capturing said output signal to provide a second output signal.
17. The method of claim 15 wherein said step of latching comprises the step of latching said input signal in at least three clocked D-type latches each having a D input terminal for receiving said input signal, a clock input terminal for receiving a clock signal, and an output terminal for providing a respective one of said at least three corresponding latched values, and having corresponding ones of said at least three different threshold voltages associated therewith.
18. The method of claim 15 wherein said step of activating said first intermediate signal comprises the step of activating said first intermediate signal using a NOR gate.

19. The method of claim 15 wherein said step of activating said second intermediate signal comprises the step of activating said second intermediate signal using an AND gate.
20. The method of claim 15 further comprising the step of performing said steps of placing said output signal in said first predetermined logic state and changing said output signal from said first predetermined logic state to said second predetermined logic state using an SR-type flip-flop.